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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/677,263 | 09/30/2000 | Xia Kevin Dai | 042390.P9724 | 2093 |

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John Patrick Ward
Blakely Sokoloff Taylor & Zafman LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1026

| EXAMINER | |
|---|---|
| YANCHUS III, PAUL B | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2116 | 15 |

DATE MAILED: 08/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/677,263 | DAI, XIA KEVIN | |
| | Examiner | Art Unit | |
| | Paul B Yanchus | 2116 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *14 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,7-11,16,18-21,29 and 31-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 7-11, 16, 18-21, 29 and 31-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

This office action is in response to communications filed on 5/14/04.

### *Response to Arguments*

Applicant's arguments filed on 4/8/04 have been fully considered but they are not persuasive.

Regarding claims 1, 7-11, 16, 18-21, 29 and 31-36, Applicant argues that Noble does not disclose or suggest the limitation "during the frequency level transition the processor is to be placed in a sleep state of and not a deep sleep state, a core processor clock remains active during the sleep state." However, Noble does disclose the limitation. Noble states that halting the operation of the processor during transitions between power modes will reduce the time taken to transition between the power modes [column 7, lines 1-9]. Therefore, Noble does disclose the limitation "during the frequency level transition the processor is to be placed in a sleep state of and not a deep sleep state, a core processor clock remains active during the sleep state."

The rejections to claims 1, 7-11, 16, 18-21, 29 and 31-36 are respectfully maintained.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 7, 9-11, 16, 19, 20, 31-32 and 34-35 are rejected under 35 U.S.C. 102(b) as being anticipated by Noble et al., US Patent no. 5,760,636.

Regarding claims, 1-7 and 9-10, Noble et al. teaches a system comprising:

a processor [column 6, lines 24-25];

a detector to detect a power management event [column 3, lines 40-52]; and

a controller to transition a first setting of the processor from a first performance mode to a second performance mode, including to raise a processor supply voltage level from a first voltage level to a second voltage level, and then to raise the processor clock frequency from a first frequency level to a second frequency level, the processor to remain in an active mode during the voltage level transition [column 6, lines 30-54], wherein during the frequency level transition the processor is to be placed in a sleep state of and not a deep sleep state, a core processor clock remains active during the sleep state [column 7, lines 1-9].

Noble et al. teaches transitioning a level of voltage supplied to a processor from a low power state to a normal power state, in response to detection of a desire to change a computer system in low power mode to normal power mode. After voltage to the processor is increased, the core clock frequency of the processor is increased from a low frequency level to a higher frequency level. Noble et al. teaches that the processor is active during the voltage level transition [column 6, lines 30-54]. Noble et al. also teaches that the processor can be placed in a sleep state [halting the operation] during a frequency transition to reduce the transition time [column 7, lines 1-9].

Regarding claims 11, 16, 19 and 20, Noble et al. teaches a system comprising:

a processor [column 8, lines 20-21];

a detector to detect a power management event [column 8, lines 20-40]; and

a controller to transition a first setting of the processor from a first performance mode to a second performance mode, including to lower a core clock frequency from a first frequency level to a second frequency level, and to lower a processor supply voltage level from a first voltage level to a second voltage level, the processor to remain in an active mode during the voltage level transition [column 8, lines 20-53], wherein during the frequency level transition the processor is to be placed in a sleep state of and not a deep sleep state, a core processor clock remains active during the sleep state [column 7, lines 1-9].

Noble et al. teaches transitioning a level of voltage supplied to a processor from a normal power state to a low power state, in response to detection of a desire to change a computer system in low power mode to normal power mode. After frequency of the processor is decreased, the supply voltage to the processor is decreased from a normal frequency level to a lower frequency level. Noble et al. teaches that the processor is active during the voltage level transition [column 8, lines 20-53]. Noble et al. also teaches that the processor can be placed in a sleep state [halting the operation] during a frequency transition to reduce the transition time [column 7, lines 1-9].

Regarding claims 31 and 32, Noble et al., as described above, teaches a system comprising a processor that changes operating states based on power management events. Therefore, Noble et al. also teaches an apparatus, which causes a processor to change operating states based on power management events.

Regarding claims 34 and 35, Noble et al., as described above, teaches a system comprising a processor that changes operating states based on power management events.

Therefore, Noble et al. also teaches an apparatus, which causes a processor to change operating states based on power management events.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8, 18, 21, 29, 33 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noble et al., US Patent no. 5,760,636, in view of Pole, II et al., US Patent no. 6,311,281.

Regarding claims 8, 18, 33 and 36, Noble teaches a system comprising a processor that changes operating states based on power management events, as described above, but does not explicitly teach detecting a power management event that includes a change of power source between an internal power source and an external power source. In summary, Noble et al. does not teach changing the operating state of a processor based on the type of power source supplying power to the system.

Pole, II et al. teaches changing the operating state of a processor based on the type of power source supplying power to the system. Pole, II et al. teaches operating a processor in a high performance state when a large amount of power is available to the processor and operating the processor in a lower performance mode when a lesser amount of power is available to the processor [column 2, lines 25-35].

It would have been obvious to one of ordinary skill in the art to, as taught by Pole, II et al., change the operating modes of a processor based on the power supplied to the system taught by Noble et al. in order to save power when system power consumption is the greatest concern or to operate faster when system performance is the greatest concern [column 2, lines 25-35].

As per claims, 21 and 29, Noble et al. and Pole, II et al. teach a system comprising a processor which changes operating states based on power management events, as described above. Therefore, Noble et al. and Pole, II et al. also teach a computer readable medium, which causes a processor to change operating states based on power management events.

***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul B Yanchus whose telephone number is (703) 305-8022. The examiner can normally be reached on Mon-Thurs 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H Browne can be reached on (703) 308-1159. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul Yanchus
July 27, 2004